19. (Amended) A module comprising:

two chips connected together according to the method of one of claims 13-17.--

## REMARKS

Reconsideration of this Application is respectfully requested in view of the remarks contained herein. This Amendment responds to the Office Action dated April 8, 2002. Claims 1-17 and 19 are pending.

Claims 1 - 19 have been rejected under the first and second paragraphs of 35 U.S.C. §112.

Claims 1-3, 6-8, and 12-19 have been rejected under 35 U.S.C. §103(a) as unpatentable over Gaul, U.S. Patent No.5,814,889.

Claims 4, 9 and 10 have been rejected under 35 U.S.C. §103(a) as unpatentable over Gaul in view of Yagi et al., U.S. Patent No. 6,215,114.

In view of the cancellation of dependent claim 18, all rejections of that claim are moot and, accordingly, are not addressed herein. In addition, it is noted that claims 5 and 11 have not been rejected over any prior art.

Claims 1-17 and 19 have been amended, either explicitly or through their dependency from an amended claim. It is respectfully submitted that, in view of the points presented below, all of the originally submitted claims were allowable over the prior art and satisfied all aspects of Section 112. However, the claims have been amended to ensure that aspects that were inherent (i.e. necessarily present in the claims) but not explicitly presented are now explicit to avoid possible similar questions being asked by others in the future, thereby eliminating the need for someone to read this Response and its direction to the Specification to obtain the answer.

It is further respectfully submitted that the pending claims, in their unamended form, distinguished over the prior art. None of the amendments made herein were made to distinguish over the cited prior art.

In addition, enclosed herewith is an Information Disclosure Statement, a Form PTO-1449 listing the references to be considered and copies of the cited references. It is respectfully requested that the references be considered and an initialed copy of the PTO-1449 be returned with the next paper.

The §112, ¶1 Rejection

The Examiner has rejected claims 1-19 under the first paragraph of 35 U.S.C. §112 as not enabled because "Claims 1 and 13 refer to 'not aligned' contacts or 'mismatched' contacts" and that the "specification does not show how such contacts are formed nor is it shown what the degree of mismatch/alignment is."

Applicants respectfully submit that "how such contacts are formed" or "the degree of mismatch/alignment" are irrelevant to the claimed invention and, accordingly, that the present invention is enabled for several reasons.

First, the procedures and/or ways contacts are formed on optical devices such as lasers, detectors, modulators, etc. are well known in the field involved in designing such devices – without such contacts the devices are unusable. The same is true for electronic chips, the design and manufacture of which having been well developed over more than the past 30 years.

Second, the present invention relates to the hybridizing of optical devices with electronic chips, not the formation of those optical devices nor the formation of the contacts on either the active device or the electronic chip – that formation is the province of the respective providers of those devices. Therein lies the problem addressed by the present invention.

The problem addressed by the present invention does not occur where two chips are merely connected, for example by wirebonds, from contact pads of one to contact pads of the other. This is because with wirebond connections, the contact pads can be anywhere. The problem does occur where two chips will be hybridized because they are joined by physically bringing the two together, particularly when one is a chip containing top active optical devices.

With top active devices, for example top active lasers (or photodetectors), light emission (or receipt) occurs on the same side as the contacts for the device. In order to hybridize the chip to an electronic chip, the device bearing chip would have to be "flipped over" so that the contacts could be mated to those on the electronic chip. However, flipping the chip over means that the emission will be into (or light receipt blocked by) the electronic chip. Thus, the top active chip orientation must be maintained.

As noted in the specification from the last paragraph of page 3 through the first full paragraph on page 5, the present invention is directed towards solving the problem of hybridizing optical devices with electronic chips that, for example, contain the drive and/or control electronics for the optical devices, and where each has electrical contacts to which the other must connect, but the contacts do not properly coincide, when the two are superimposed.

In that portion of the specification, and as shown in FIGS. 3 and 4, unless the placement location for the contacts on the optical devices and the contact pad locations on the electronic chip to which they will be connected are designed to coincide, i.e. they will properly correspond in location when superimposed and brought together, proper hybridization of the two will not be possible. In other words, if each does not take into account the contact placement of the other a lack of correspondence between their respective contacts will likely result (i.e. they will be "not aligned" or are "mismatched").

The above referenced portion of the specification further notes that it is also desirable to be able to procure the optical devices from one or more vendors and/or the electronics from one or more other vendors. Each such vendor may have placed the contacts for their respective devices in different places. Despite this fact, the teachings of the present invention make it possible for those optical devices and electronic chips to be hybridized without regard for where the particular vendors have placed the electrical contacts on their respective products.

Fourth, the "degree of mismatch/alignment" is also largely irrelevant because it will depend upon the placement of the contacts on a particular optical device relative to the placement of the contacts on the particular electronic chip to which the optical device will be joined. As shown in FIGS. 16, 17 and 18 and described, *inter alia*, from the first full paragraph on page 21 through the top two lines of page 28 of the present specification, the technique is the same whether the mismatch is small or relatively large so the degree of mismatch/misalignment is irrelevant (ignoring, of course, where the contacts or makeup of either or both are such that the mismatch prevents hybridization altogether).

Accordingly, it is respectfully submitted that, in view of the above, the rejection of claims 1-19 under the first paragraph of 35 U.S.C. §112 should be withdrawn.

The §112, ¶2 Rejections

The Examiner has rejected claims 1-19 under the second paragraph of 35 U.S.C. §112 as indefinite based upon three items, labeled herein a), b) and c) for convenience:

a) The Office Action states that "Claim 1 shows 'points' that are coincident with the active device contacts but claim 6 states that connecting comprises traces" and "it is not understood how the traces can connect to these points";

b) The Office Action states that "Claim 10 refers to a thickness greater than a minimum lasing thickness" but does not provide what it is; and

c) The Office Action states that "it is not understood what the not aligned/mismatch [of claims 1 and 13] is."

It is respectfully submitted that the rejected claims are definite, as demonstrated below, where each of items a), b) and c) are addressed in turn.

**ITEM a)**

As to the first item, labeled a) above, it is respectfully submitted that in both claim 1 and claim 6 the term "points" is definite, since it is merely a synonym for, and refers to, locations (i.e. the locations on the substrate beneath the device contacts.

As set forth in claim 1, the electrically conductive sidewalls extend from the active device contacts through the substrate to points (i.e. locations) on the bottom of the substrate substantially coincident with the active device contacts. In other words, if the substrate was transparent or a slice was made through the device along the length of the opening such that each of the contacts on the top and the "points" where the openings reach the bottom of the substrate could be seen, the two would be substantially coincident as shown, for example, in FIGS. 16 and/or 17. Those points (i.e. locations) are therefore extensions of the active device contacts through the substrate and consequently, since the active device contacts and the electronic chip contacts are not aligned, the locations and the electronic chip contacts will still not physically not coincide. The "connecting" provides the bridge between the locations on the substrate and the electronic chip contacts, the necessary result of which is the creation of electrically conductive physical connections between "each of the at least some active device contacts" and their respective "electrically corresponding chip contact".

Claim 6 further defines what is involved in the "connecting" recited in claim 1, namely "the connecting comprises: patterning traces between the points [i.e. the locations on the substrate] and the electronic chip contacts, and making the traces electrically conductive."

It is respectfully submitted that claim 1 and all claims depending therefrom are definite and particularly point out and claim what applicants regard as the invention. To the extent the rejection is based upon item "a)", in view of the above remarks, withdrawal of the rejection is requested.

**ITEM b)**

As to claim 10, the Examiner has asked what the minimum lasing thickness is. It is respectfully submitted that it is dependent upon the particular laser. As noted in the specification at pages 28 (last full paragraph) through page 29 (first full paragraph):

> Although different types of laser devices will require a different specific thickness, the thickness of the substrate should be at least several times as large as the thickness of the laser cavity, in the case of DFBs and DBRs and the distance between the mirrors, in the case of VCSELs. Since the precise distance will vary from device to device, a good rule of thumb is to use a factor of 10X the thickness of the laser cavity. However, if the thickness can be controlled precisely, it can be less than the 10X factor, the particular minimum thickness being empirically ascertainable as the minimum thickness where the AR coating does not affect the laser's ability to lase.
>
> An analogous approach can be used for topside active lasers. In the case of topside active lasers, a substrate (which can be the carrier noted above, a separate substrate applied after carrier removal, or, if contact rerouting is not necessary or performed on the other chip, instead of a carrier) is attached to the topside of the lasers. The substrate is either thinned, after application, to a thickness as noted above, [or] thinned to such thickness prior to application.

It is further respectfully submitted that, in view of the above, claim 10 is also definite and particularly points out and claims what applicants regard as the invention. Withdrawal of the rejection, to the extent it is based upon item "b)", is requested.

**ITEM c)**

The Examiner has further noted with respect to claims 1 and 13 "it is not understood what the not aligned/mismatch is. Is there a specific number?"

It is respectfully submitted that the remarks provided above with respect to claim 1 provides the answer to the question posed. In short, the non-alignment/mismatch relates to the location of the contacts on the particular optical device relative to the contacts on the electronic chip to which that device must connect when hybridized and is therefore dependent upon the particular optical device and electronic chip being hybridized.

As to claim 13, it is respectfully submitted that the "not aligned/mismatch" is the same as described in connection with claim 1. In order to ensure that this is clear, the preamble of claim 13 has been amended to now read "A method of connecting two chips, one of which being a topside active chip, each of the two chips having electrically corresponding contacts to be joined together that are physically mismatched in alignment relative to each other, the method comprising: . . ."

The question "Is there a specific number?" is not understood. Is there a specific number of what? Number of mismatches, amount of misalignment, or something else. To try to answer the question, the answer is believed to be no, irrespective of whether the question relates to the first two – there are no particular number of mismatches nor amount of misalignment. Depending upon the particular case, all of the contacts on the two items to be joined may be physically non-aligned/mismatched, one or more contacts on each may be aligned while others may be non-aligned/mismatched.

For hybridizing topside active devices in accordance with the teachings of the present invention, due to the side of the device the contacts are on, even if the contacts between the two

chips are perfectly aligned there is need to resort to the invention. As the contacts between two chips are more misaligned, the benefits achievable with the invention increase.

It is therefore further respectfully submitted that, in view of the above, claim 13 is also definite and particularly points out and claims what applicants regard as the invention. Withdrawal of the rejection, to the extent it is based upon item "c)", is requested.

It is therefore respectfully submitted that all of claims 1-19 are definite and withdrawal of the rejection under the second paragraph of 35 U.S.C. §112 be withdrawn.

It is respectfully noted that claims 5 and 11 were not subject to an art rejection. As a result, since the Section 112 rejections have now been overcome, allowance of those claims is solicited.

The Prior Art Rejections

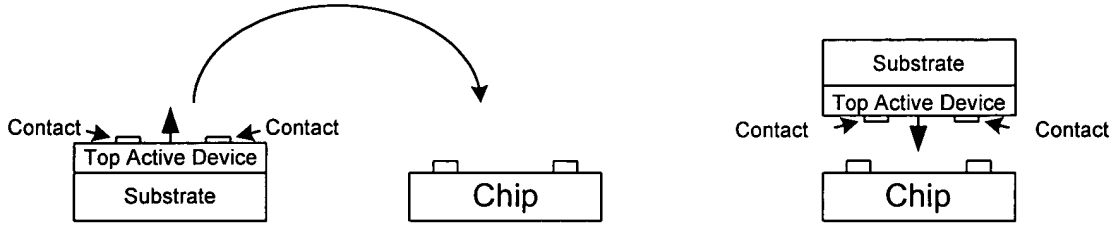
Claims 1-3, 6-8, and 12-19 have been rejected under 35 U.S.C. §103(a) as unpatentable over Gaul, U.S. Patent No.5,814,889 (hereafter "Gaul").

It is respectfully submitted that there are significant differences between the Gaul reference and the rejected claims.

As the Office Action recognized, Gaul shows a method of interconnecting two chips using an intermediate chip or interposer (Interposer). Contacts of one of the two chips in Gaul are brought into contact with one side of the Interposer and contacts of the other chip are brought into contact with the other side of the Interposer, thereby connecting the two chips.

In contrast, all of the claims relate to hybridizing a top active chip, having its contacts on the top side, with another chip. As noted above, the top active nature of the chip means that the device contacts are on the same side that the device emits or receives light from. As a result, the contacts of each can not merely be brought together, with or without a Gaul-like Interposer,

because if it were done, the active side of the top active chip would be between the two chips, rendering it useless as shown below.




Moreover, there is no teaching of suggestion in Gaul or any of the cited references of applicants' invention as claimed, whether or not Gaul has metal lined vias.

These aspects are reflected in the claims and are not implicated by the amendments.

Moreover, although stated slightly differently but of identical intended scope, claim 1 in both original unamended and now amended form points out that the openings defined by the sidewalls extend from the device contacts to the bottom of the substrate. Inherently this can only mean through the substrate. This aspect is also lacking from Gaul, and there is no teaching or suggestion otherwise in any of the cited art.

It is respectfully submitted that claim 1 is allowable and early, favorable action in that regard is solicited.

Claims 2, 3 and 6-8 all depend from claim 1. Accordingly, those claims are also allowable based upon their dependence from an allowable claim.

Amended independent claim 12 is similarly allowable because it specifically requires a top active device. Accordingly the above explanation and distinctions apply with equal force to claim 12.

It is respectfully submitted that amended claim 12 is allowable and early, favorable action in that regard is solicited.

Amended independent claim13 also recites connecting two chips "one of which being a topside active chip". Thus, claim 13 is similarly distinguishable from Gaul. In addition, claim 13 has also been amended so that it is clear that the "insulator" is part of the topside active chip (i.e. its substrate) and hence, now explicitly states that the conductive paths extend "from the device contacts through the topside active chip". Accordingly, this is a further independent distinction between claim 13 and Gaul.

It is respectfully submitted that amended claim 13 is allowable and early, favorable action in that regard is solicited.

Claims 14-18, all depend from claim 13. Accordingly, those claims are also allowable based upon their dependence from an allowable claim.

Claim 19 as amended depends from claims 13-17. By virtue of that dependency, claim 19 is allowable for the same reasons.

Accordingly, it is respectfully submitted that the invention as defined by claims 1-3, 6-8 and 12-13 are all allowable over Gaul.

Claims 4, 9 and 10 have been rejected under 35 U.S.C. §103(a) as unpatentable over Gaul in view of Yagi et al., U.S. Patent No. 6,215,114 (hereafter "Yagi").

First, it is respectfully noted that each of claims 4, 9 and 10 depend from allowable claim 1 and Yagi does not supply, suggest or provide motivation that would remedy the deficiencies of Gaul. Accordingly, each of those claims is allowable.

Moreover, Yagi relates to the art of near field microscopy that is used to allow viewing of features smaller than the wavelength of the illuminating light. This reference is from a different

field than the present invention, it is used for a different purpose and there is no teaching or suggestion to combine Yagi with Gaul in such a manner as would achieve the invention claimed in claims 4, 9 or 10.

The Office Action states that that it would have been obvious to "apply the Gaul technique to attach Yagi et al. structure to provide processing/drive circuitry." Applicants respectfully disagree. The referenced portions of Yagi have nothing to do with the processing and drive circuitry for the detectors (FIG. 3) or the lasers (FIG. 4) of Yagi and applicants can not identify any teaching or suggestion in Yagi or Gaul that would lead one to combine the two and achieve the claimed invention, notwithstanding the fact that the two have nothing to do with each other as a practical matter.

Claim 4 recites "attaching a carrier to the top active device". Yagi does not do this. The device of FIG. 2H does not touch items 621, 622 or 623 of FIG. 3 or 721, 722 or 723 of FIG. 4.

Accordingly, claim 4 is allowable for this independent reason.

Claim 9 recites "thinning the substrate". Yagi does not do this. The relevant substrate of Yagi is part of 620 of FIG. 3 or 720 of FIG. 4.

Accordingly, claim 9 is allowable for this independent reason.

Claim 10 recites "attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device." Yagi does not do this. In Yagi, there is no carrier over the top active device, there is only a hole. It is that hole through which light enters (611 of FIG. 3) or light is emitted (711 of FIG. 4).

Accordingly, claim 10 is allowable for this independent reason.

It is respectfully submitted that, in view of the above, all claims are patentable over the prior art and early and favorable action in that regard is solicited.

## CONCLUSION

Based on the foregoing remarks, it is respectfully submitted that all the claims as currently pending are patentable and in condition for allowance. Reconsideration of the rejections and allowance of the claims are therefore respectfully requested.

If the Examiner believes that any of the pending claims present any issues which could be resolved by a further telephone interview, the Examiner is respectfully urged to telephone the undersigned's direct line at (212) 415-8500. Alternatively, the undersigned may be contacted by e-mail at rstraussman@morganfinnegan.com.

The Commissioner is hereby authorized to charge any additional fees which may be required for consideration of this amendment on the merits, or credit any overpayment to Deposit Account No. 13-4500, Order No. 4024-4021.

A DUPLICATE COPY OF THIS SHEET IS ATTACHED.

Respectfully submitted,

MORGAN & FINNEGAN

Dated: September 9, 2002 By: _____

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# APPENDIX

**NOTE:** Additions are denoted with underlining and deletions are denoted with square brackets.

1. (Amended) A method of creating a hybridized chip combining [using] a top active optical device chip, having a substrate including a first side and active device contacts on top active devices located on the first side, the top active optical devices also being on the first side, [combined] with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

creating sidewalls defining openings in the substrate[,] extending from the active device contacts on the first side [at the active device contacts] through the substrate to a bottom side of the substrate opposite the first side[,] at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some [and the] electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

5. (Amended) The method of claim 4 further comprising:

removing the carrier after the connecting [the points and the electronic chip contacts].

6. (Amended) The method of claim 1 wherein the connecting comprises:

patterning traces between the points and the locations correspondingly aligned with the at least some electronic chip contacts, and

making the traces electrically conductive.

7. (Amended) The method of claim 6 wherein the patterning traces comprises:

patterning at least some of the traces on the substrate and at least some other of the traces on the electronic chip.

8. (Amended) The method of claim 6 wherein the patterning traces further comprises:

patterning [the] traces on the electronic chip.

13. (Amended) A method of connecting two chips, one of which being a topside active chip, each of the two chips having electrically corresponding contacts to be joined together that are physically mismatched in alignment relative to each other, the method comprising:

creating electrically conductive paths on an insulator surface of the topside active chip, each of the electrically conductive paths extending between physical locations of device contacts of one of the two chips and physical locations of the electrically corresponding contacts on the other of the two chips, from the device contacts through the topside active chip to the physical locations of the electrically corresponding contacts.

14. (Amended) The method of claim 13 wherein the insulator has holes defined by sidewalls, extending from the device contacts through the insulator, and the creating the electrically conductive paths comprises:

making the holes electrically conductive.

17. (Amended) The method of claim 13[, wherein the insulator is part of one of the two chips, the method] further comprising:

joining [the other of] the two chips [to the insulator].

19. (Amended) A module comprising:

two chips connected together according to the method of one of claims 13-[18] 17.